FireSim and Chipyard Tutorial: Intro

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Presenters/Organizers

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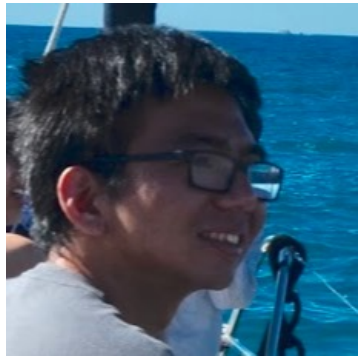
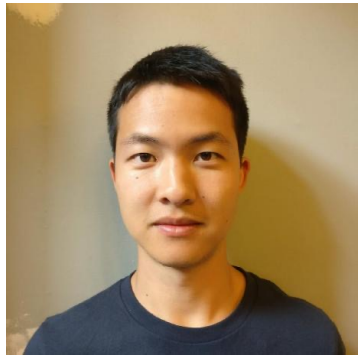


Jerry Zhao



Harrison Liew

Abraham Gonzalez

James Dunn

Nathan Pemberton

Albert Ou

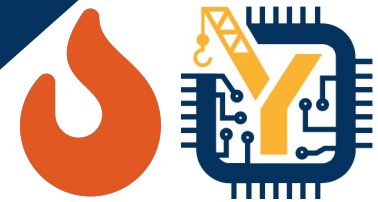
David Biancolin

Borivoje Nikolić

Krste Asanović

Berkeley Architecture Research

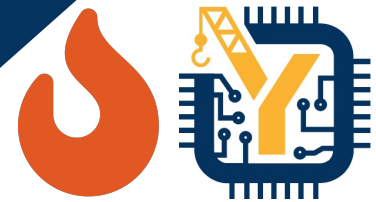
A *Golden Age* in Computer Architecture



- No more traditional scaling…
- An architect's dream: everyone wants custom microarchitectures and HW/SW co-designed systems
- Also, a golden age to have *direct impact* as researchers
  - Exploding open-source hardware environment
  - An open-ISA that can run software we care about

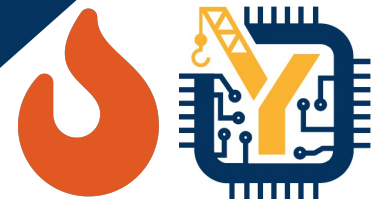
https://cacm.acm.org/magazines/2019/2/234352-a-new-golden-age-for-computer-architecture/fulltext

A *Dark Age* in Computer Architecture tools



- What do we need to do good architecture research?
  - Need tools that let us evaluate designs on a variety of metrics:
    - Functionality
    - Performance
    - Power
    - Area
    - Frequency
  - Especially in small teams (grad students, startups), these tools need to be *agile*
  - Historically, without good open IP, had to build abstract arch/uarch simulators out of necessity
    - But now, we have much better IP and software compatibility, so what's stopping us?

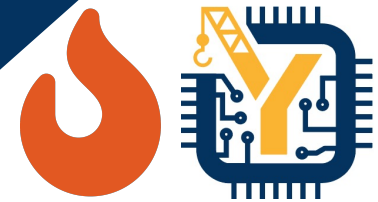
A *Dark Age* in Computer Architecture tools



- Designed to be operated by hundreds of engineers
- Not, 10s of engineers or 1s-10s of grad students

- Two hard questions:
  - Where do I get a collection of well-tested hardware IP + complex software stacks that run on it?
  - How do I quickly obtain performance measurements for a novel HW/SW system?

Two hard questions, answered!



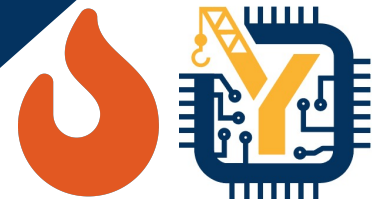
- Where do I get a collection of well-tested hardware IP + complex software stacks that run on it?

- How do I quickly obtain performance measurements for a novel HW/SW system?

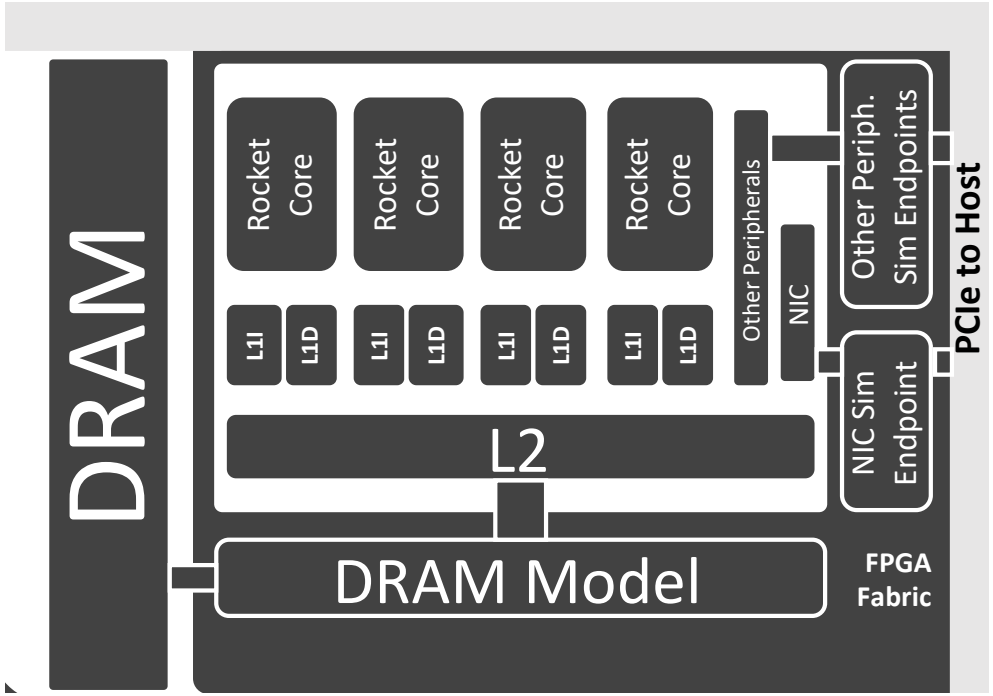
What can I do with these tools?

Measure Functionality, Performance, Power, Area, Frequency *for real HW/SW systems*, quickly and easily, with small teams of engineers

What kinds of designs can I work with?

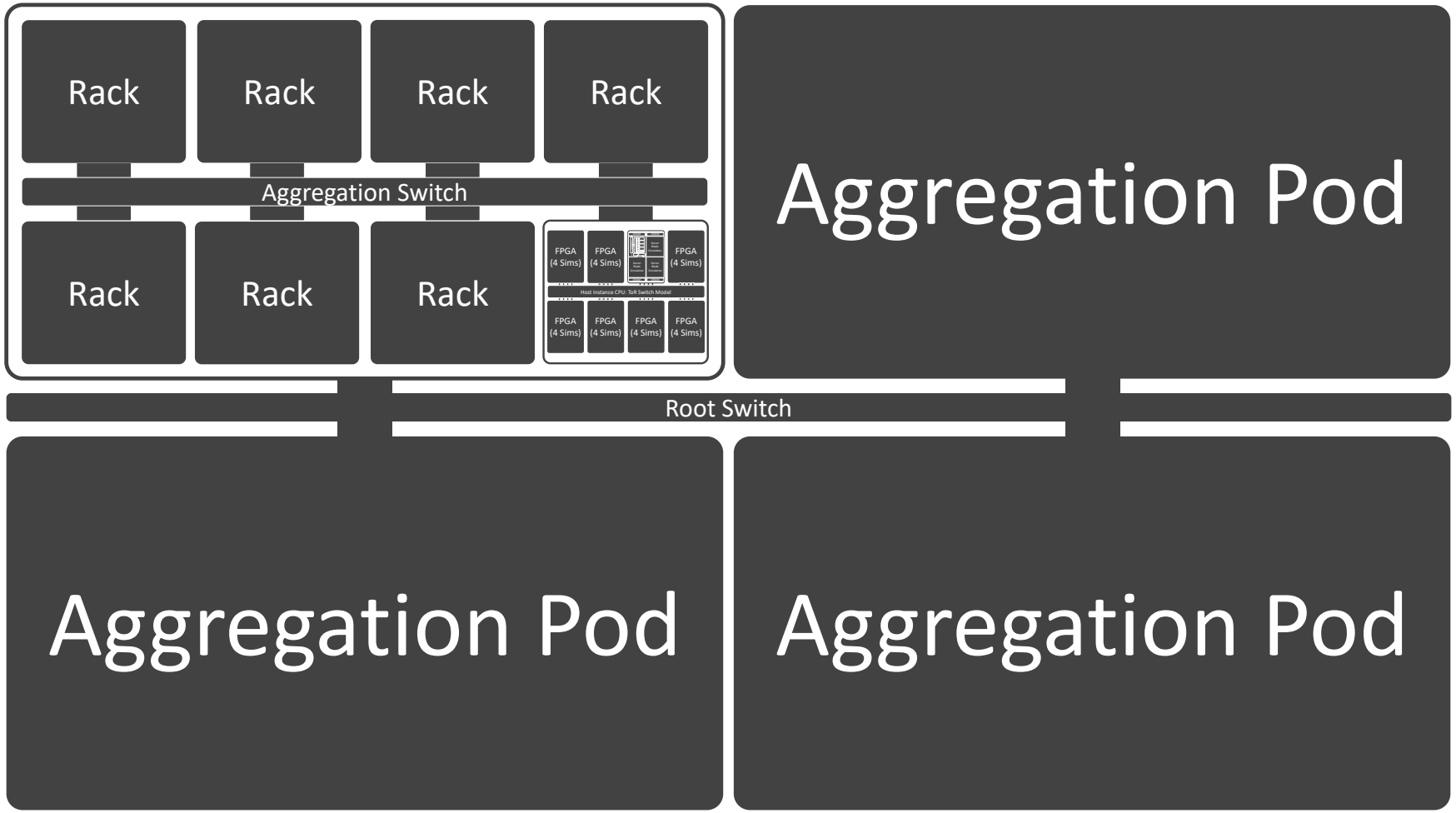


- RISC-V Cores:
  - Rocket Chip In-Order core, industry proven
  - SonicBOOM Out-of-Order Superscalar core
- Accelerators
  - Hwacha Vector Accelerator
  - sha3 accelerator
  - NVDLA (NVIDIA Deep Learning Accelerator)
  - ML Accelerators (Gemmini)
- Peripherals/other IP
  - L2 Cache, UART, Disk, Ethernet NIC, etc.
- FPGA-Simulation Models
  - Large LLCs, large DDR3 memory systems



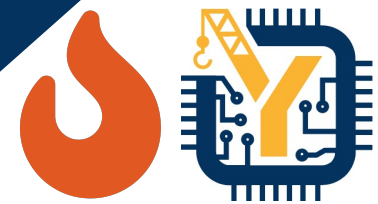
Single SoC System

What kinds of designs can I work with?



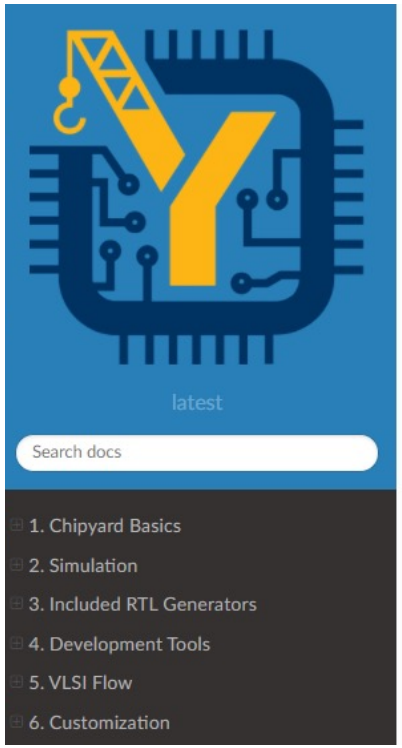
Ethernet-Networked 1024 SoC System

Chipyard is Community-Friendly



Documentation:

- https://chipyard.readthedocs.io/en/dev/
- 133 pages
- Most of today's tutorial content is covered there

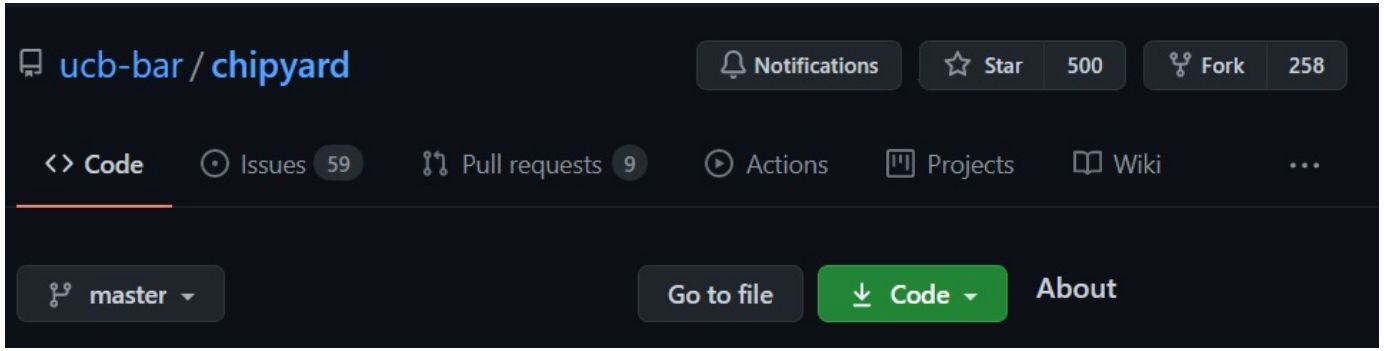


Mailing List:

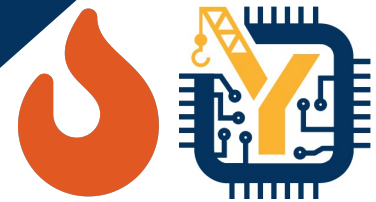
- google.com/forum/#!forum/chipyard

Open-sourced:

- All code is hosted on GitHub
- Issues, feature-requests, PRs are welcomed



Growing FireSim Community!



- Companies publicly announced using FireSim
  - Esperanto Maxion ET
  - Intensivate IntenCore
  - SiFive validation paper @ VLSI'20
- Chipyard integration
- Projects with public FireSim support
  - Rocket Chip, BOOM
  - Hwacha Vector Accelerator
  - Keystone Secure Enclave
  - NVIDIA Deep Learning Accelerator (NVDLA)
    - https://devblogs.nvidia.com/nvdla/
  - BOOM Spectre replication/mitigation
  - More in-progress! PR yours!
- Many academic users
  - ISCA '18: Maas et. al. HW-GC Accelerator (Berkeley)
  - MICRO '18: Zhang et. al. "Composable Building Blocks to Open up Processor Design" (MIT)
  - RTAS '20: Farshchi et. al. BRU (Kansas)
  - EuroSys '20: Lee et. al. Keystone (Berkeley)
  - OSDI '21: Ibanez et. al. nanoPU (Stanford)
  - See FireSim website for more!
- Education
  - Berkeley CS152/252
  - CCC/RV Summit tutorials
  - MICRO 2019 full-day tutorial
- More than 100 mailing list members
- More than 300 unique cloners per week

*FireSim ISCA'18 paper selected as an **IEEE Micro Top Pick of 2018 Arch. Confs** and as the **CACM Research Highlights Nominee from ISCA'18***

Hot off the presses @ MICRO 2021!

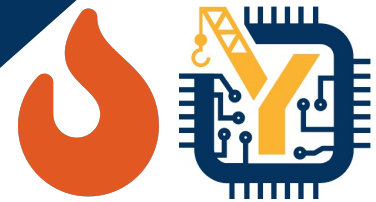
MICRO-54 Best Paper Runner-up uses FireSim and BOOM!

TIP: Time-Proportional Instruction Profiling
Bjorn Gottschall (Norwegian University of Science and Technology); Lieven Eeckhout (Ghent University); Magnus Jahre (Norwegian University of Science and Technology)

MICRO-54 Distinguished Artifact Winner uses FireSim, Chipyard, and BOOM!

A Hardware Accelerator for Protocol Buffers
Sagar Karandikar (UC Berkeley, Google); Chris Leary, Chris Kennelly (Google); Jerry Zhao, Dinesh Parimi, Borivoje Nikolic, Krste Asanovic (UC Berkeley); Parthasarathy Ranganathan (Google)

Today's Agenda



10:00: Introduction, logistics, etc. – Sagar
10:05: Chipyard Basics – Jerry
10:35: Customizing the SoC – Jerry
11:05: Integrating Verilog Designs in Chipyard - Abe
11:15: Coffee break
11:25: Hammer VLSI flow – Harrison
11:55: FPGA Prototyping – James
12:25: FireSim Introduction – Sagar
12:55: Lunch
13:45: FireSim – Building Hardware Designs - David
14:15: FireSim – Building Software Workloads - Nathan
14:45: Running a FireSim Simulation: Simulating the SHA3 w/Linux - Albert
15:15: Coffee break
15:25: Debugging and Profiling a FireSim-simulated design - Abe
15:50: Conclusion - Abe