

FireSim and Chipyard Tutorial: Welcome!

You must enter a valid email on this form! →

1. Fill out the form at [in-person only] now for EC2 instance access

Then

2. You'll receive two emails. Follow insts to login, then wait.



Berkeley
Architecture
Research



FireSim and Chipyard Tutorial: Intro

Sagar Karandikar

UC Berkeley

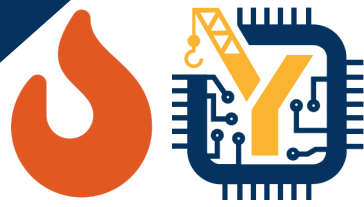
sagark@eecs.berkeley.edu



Berkeley
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Research



Presenters/Organizers



Sagar
Karandikar



Jerry
Zhao



Nayiri
Krzysztofowicz



Albert
Ou



Abraham
Gonzalez



Sophia
Shao



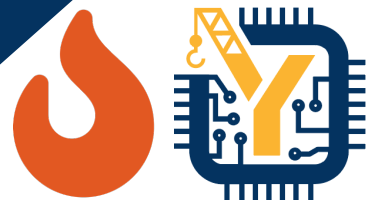
Bora
Nikolić



Krste
Asanović



Getting Started/Logistics (recap)



- Fill out the form at **[in-person only]** now for EC2 instance access
- You'll receive two emails. One from Google Forms and one that looks like →
- Follow the instructions in this one to login to your FireSim manager instance, then wait

FireSim/Chipyard Tutorial User Info Inbox x



FireSim Tutorial User Registration <mailgun@mg.sagark.org>
to sagark ▾

6:15 AM (1 minute ago)



Reply



Welcome to the FireSim/Chipyard tutorial!

Your Instance IP is 3.86.98.198

Your Instance Username is centos

There are two steps to login:

1) Save the attached key. You will likely need to fix permissions on it like so:

```
chmod 0600 tutorial-user-0000-us-east-1.pem
```

2) Next, there are two options for logging in, choose one. Mosh is highly recommended for easy persistent connections:

2a) If you have mosh installed (or can install it) we highly recommend logging in with mosh. See mosh install instructions here: <https://mosh.org/#getting>

Once installed, to login with mosh, run:

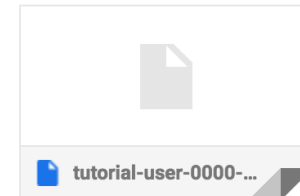
```
mosh --ssh="ssh -i tutorial-user-0000-us-east-1.pem" centos@3.86.98.198
```

2b) If mosh is not available, login with a regular ssh client, then run screen once you're on the instance:

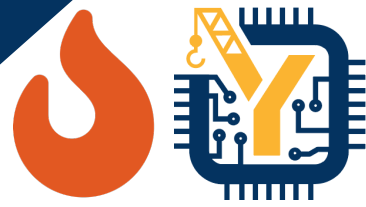
```
ssh -i tutorial-user-0000-us-east-1.pem centos@3.86.98.198
```

[now, start a screen on the remote instance]

Please let a presenter know if you have issues logging in.



A *Golden Age* in Computer Architecture



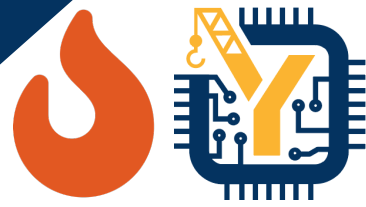
- No more traditional scaling...
- An architect's dream: everyone wants custom microarchitectures and HW/SW co-designed systems
- Also, a golden age to have *direct impact* as researchers
 - Exploding open-source hardware environment
 - An open-ISA that can run software we care about



<https://cacm.acm.org/magazines/2019/2/234352-a-new-golden-age-for-computer-architecture/fulltext>



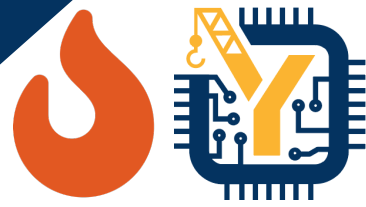
A *Dark Age* in Computer Architecture tools



- What do we need to do good architecture research?
 - Need tools that let us evaluate designs on a variety of metrics:
 - Functionality
 - Performance
 - Power
 - Area
 - Frequency
 - Especially in small teams (grad students, startups), these tools need to be *agile*
 - Historically, without good open IP, had to build abstract arch/uarch simulators out of necessity
 - But now, we have much better IP and software compatibility, so what's stopping us?



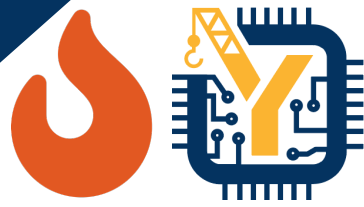
A *Dark Age* in Computer Architecture tools



- Designed to be operated by hundreds of engineers
- Not, 10s of engineers or 1s-10s of grad students
- Two hard questions:
 - Where do I get a collection of well-tested hardware IP + complex software stacks that run on it?
 - How do I quickly obtain performance measurements for a novel HW/SW system?



Two hard questions, answered!



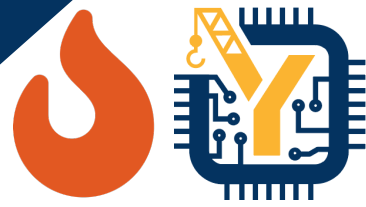
- Where do I get a collection of well-tested hardware IP + complex software stacks that run on it?



- How do I quickly obtain performance measurements for a novel HW/SW system?



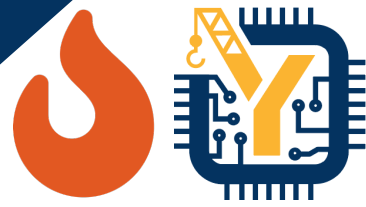
What can I do with these tools?



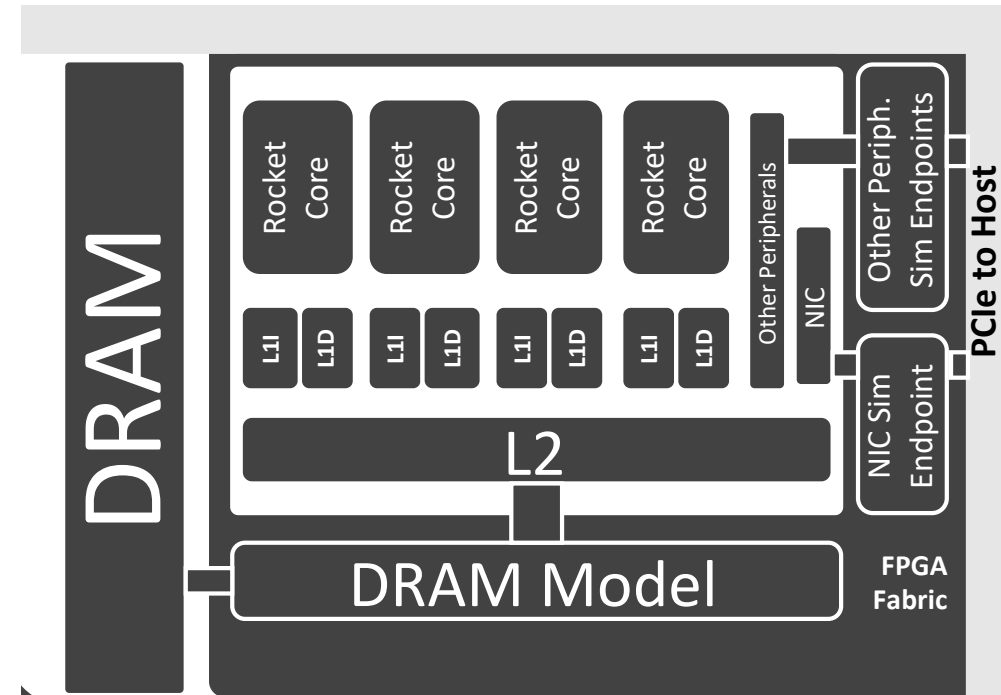
**Measure Functionality, Performance, Power,
Area, Frequency** *for real HW/SW systems,*
quickly and easily, with small teams of engineers



What kinds of designs can I work with?



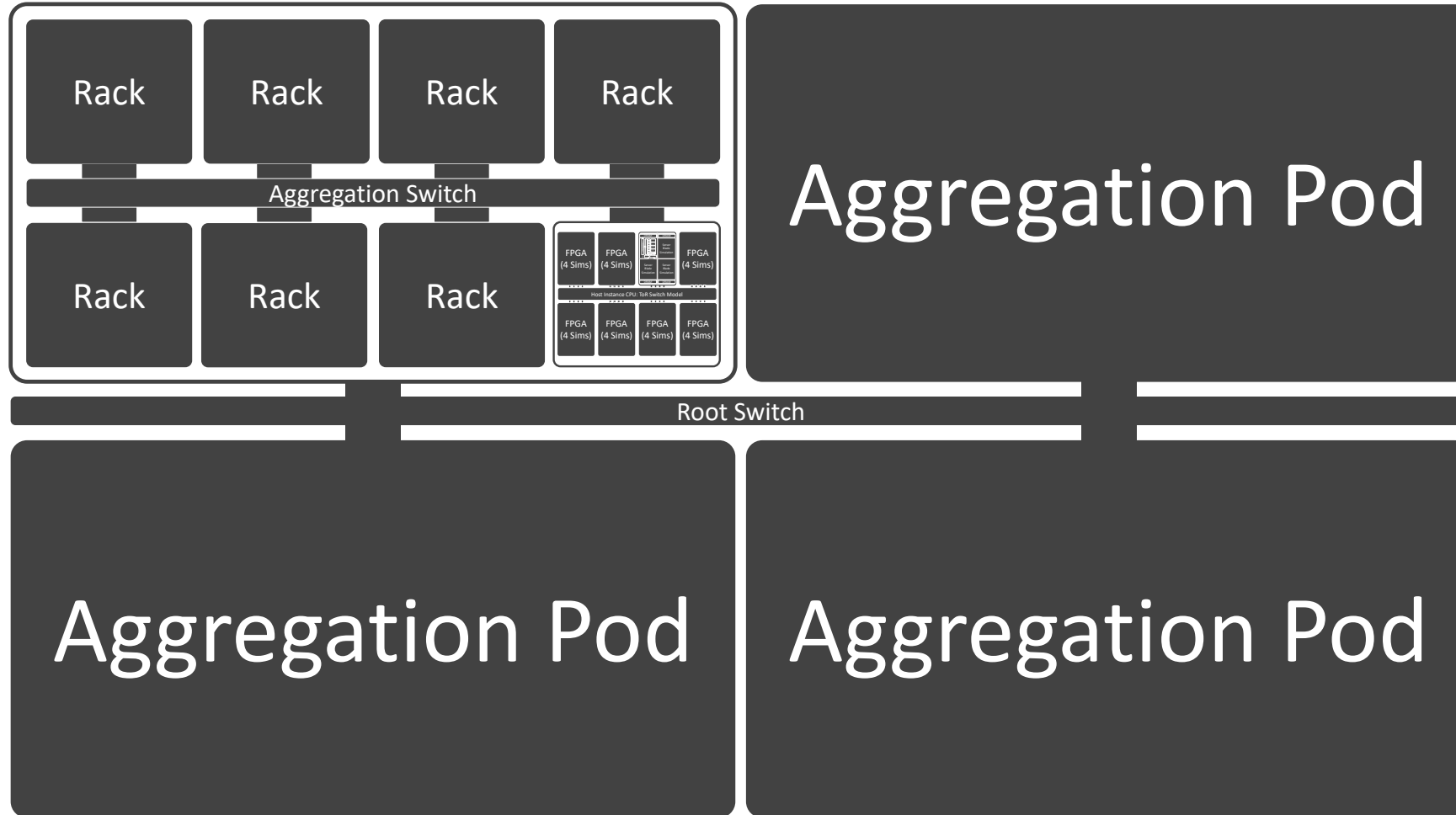
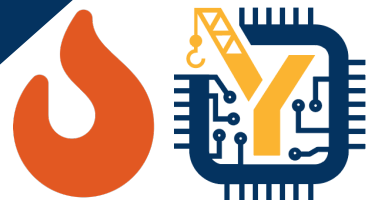
- RISC-V Cores:
 - Rocket Chip In-Order core, industry proven
 - SonicBOOM Out-of-Order Superscalar core
 - CVA6
 - Ibex
- Accelerators
 - Hwacha Vector Accelerator
 - sha3 accelerator
 - NVDLA (NVIDIA Deep Learning Accelerator)
 - Gemmini (Berkeley DNN Accelerator)
 - FFT Generator
- Peripherals/other IP
 - L2 Cache, UART, Disk, Ethernet NIC, etc.
- FPGA-Simulation Models
 - Large LLCs, large DDR3 memory systems



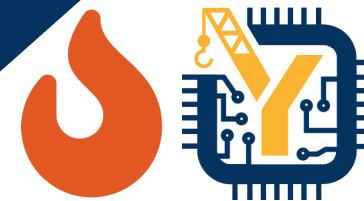
Single SoC System



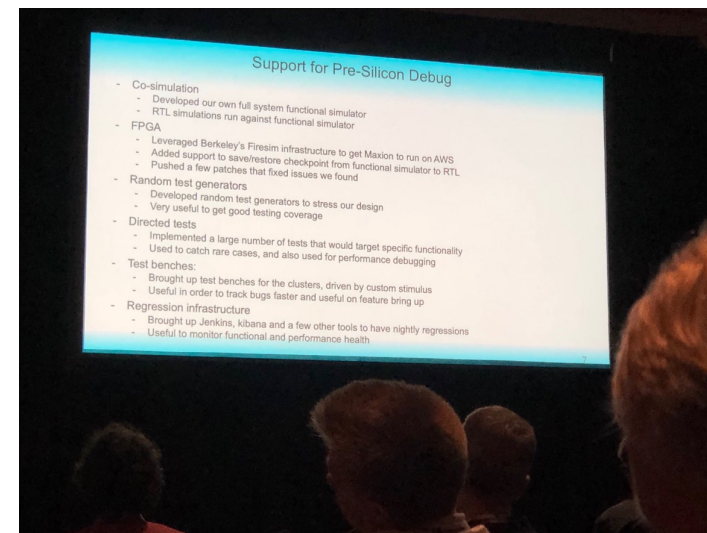
What kinds of designs can I work with?



Join the FireSim Community! Open-source users and industrial users



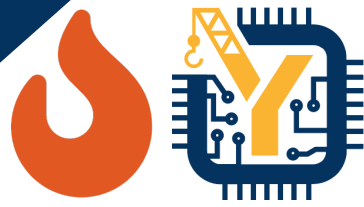
- More than 150 mailing list members and 500 unique cloners per-week
- Projects with public FireSim support
 - Chipyard
 - Rocket Chip
 - BOOM
 - Hwacha Vector Accelerator
 - Keystone Secure Enclave
 - Gemmini
 - NVIDIA Deep Learning Accelerator (NVDLA):
 - NVIDIA blog post: <https://devblogs.nvidia.com/nvdl/>
 - BOOM Spectre replication/mitigation
 - Protobuf Accelerator
 - Too many to list here!
- Companies publicly announced using FireSim
 - Esperanto Maxon ET
 - Intensivate IntenCore
 - SiFive validation paper @ VLSI'20
 - Galois and Lockheed Martin (DARPA SSITH/FETT)



Esperanto announcement at RISC-V Summit 2018



Join the FireSim Community! Academic Users and Awards

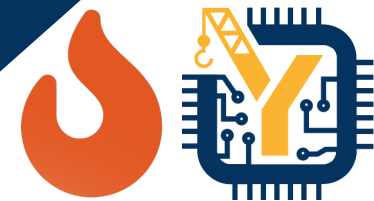


- **ISCA '18**: Maas et. al. HW-GC Accelerator (**Berkeley**)
- **MICRO '18**: Zhang et. al. “Composable Building Blocks to Open up Processor Design” (**MIT**)
- **RTAS '20**: Farshchi et. al. BRU (**Kansas**)
- **EuroSys '20**: Lee et. al. Keystone (**Berkeley**)
- **OSDI '21**: Ibanez et. al. nanoPU (**Stanford**)
- **CCS '21**: Ding et. al. “Hardware Support to Improve Fuzzing Performance and Precision” (**Georgia Tech**)
- Too many to list here: see FireSim website for more!
 - <https://fires.im/publications/#userpapers>

- Awards: FireSim ISCA '18 paper:
 - IEEE Micro Top Pick
 - CACM Research Highlights Nominee from ISCA '18
- Awards: FireSim users:
 - ISCA '18 Maas et. al.:
 - IEEE Micro Top Pick
 - MICRO '18 Zhang et. al.:
 - IEEE Micro Top Pick
 - MICRO '21 Gottschall et. al.:
 - MICRO-54 Best paper runner-up
 - MICRO '21 Karandikar et. al.:
 - MICRO-54 Distinguished Artifact winner
 - IEEE Micro Top Pick Honorable Mention
 - DAC '21 Genc et. al.:
 - DAC 2021 Best Paper winner



Join the FireSim Community! Academic Users and Awards



- **ISCA '18:** Maas et. al. HW-GC Accelerator (Berkeley)

- **MICRO '18:** Zhang et. al. "Composable Building Blocks to Optimize FPGA Accelerators"

- **RTAS '20:** F...

- **EuroSys '20:** F...

- **OSDI '21:** Ib...

- **CCS '21:** Di... Improve Fuz... (Georgia Te...

- Too many to list here: see FireSim website for more!

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- CACM Research Highlights Nominee

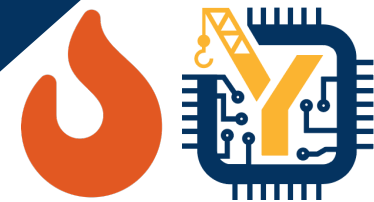
FireSim has been used in published work from authors at over 20 academic and industrial institutions*

**actually used, not only cited*

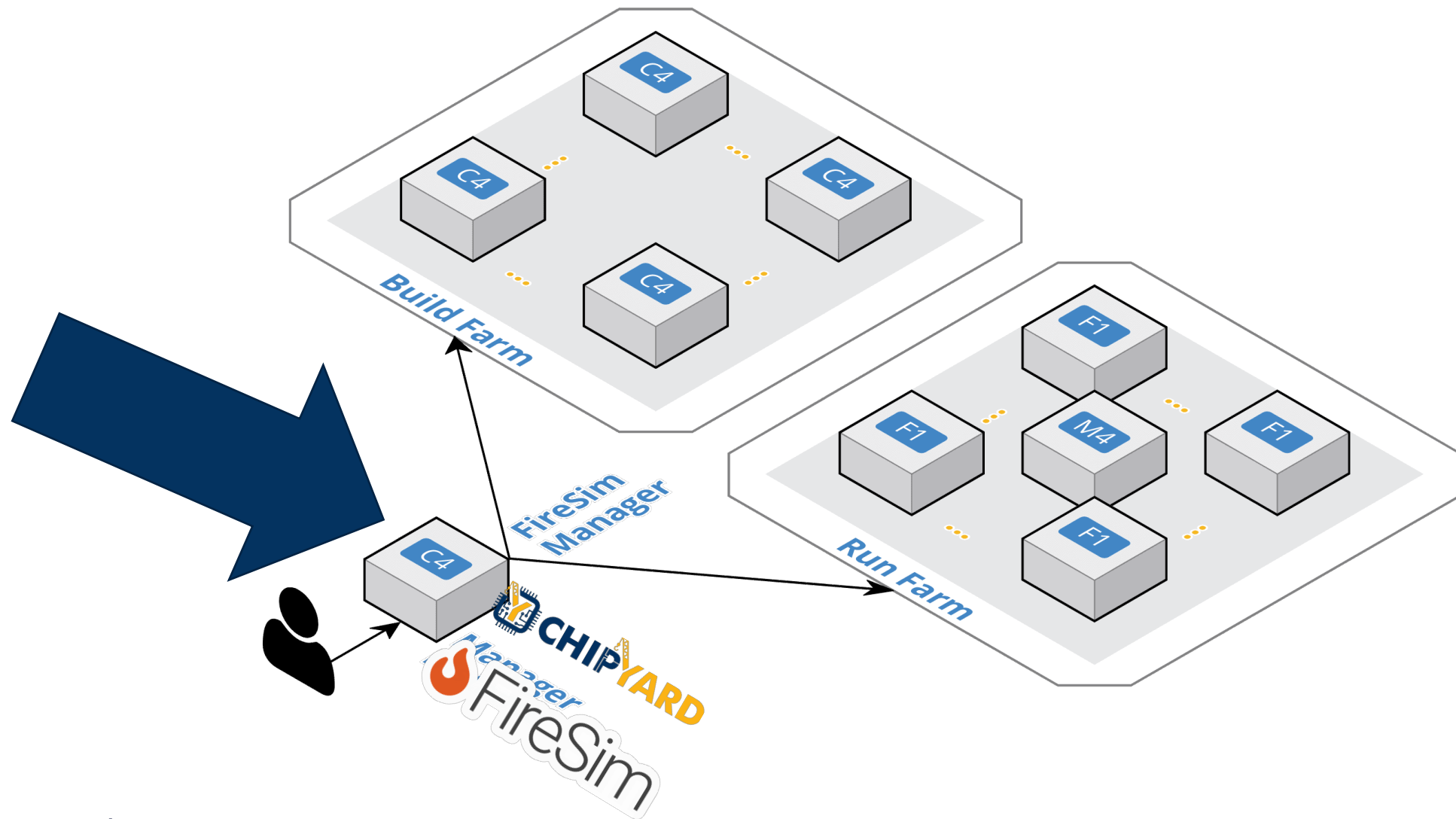
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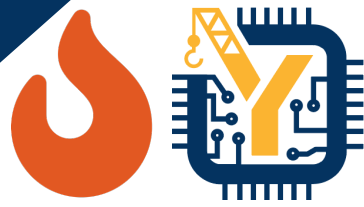
Today's Logistics



You are
here



Running a FireSim FPGA Build



- This will take a while, so we will run this in the background:

```
tmux new -s fpgabuild # this will give you a persistent  
                      # session you can reattach to
```

```
firesim managerinit --platform f1
```

[When prompted, enter your email address to get a build completion notification]

```
# runs the HW build, all the way to AGFI
```

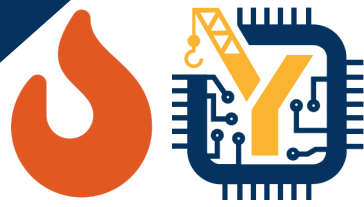
```
firesim buildbitstream
```

[Lastly, detach from tmux with “ctrl-b d”. We will return to this build later.]

[this will build a design called firesim_rocket_singlecore_no_nic_l2_lbp]



Today's Agenda - AM



8:30am: Introduction/Overview, Amazon EC2 Instance Setup, Logistics - Sagar

9:00am: Chipyard Basics – Jerry

9:30am: Building Custom RISC-V SoCs in Chipyard - Jerry

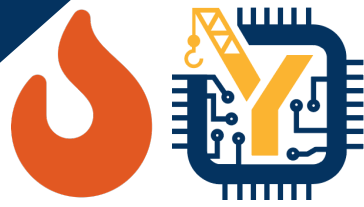
10:30am: Coffee break

11:00am: Hammer VLSI flow - Nayiri

11:30am: FPGA Prototyping - Nayiri

12:00pm - 1:30pm: Lunch

Today's Agenda - PM



1:30pm: FireSim Introduction - Sagar

2:00pm: Building Hardware Designs in FireSim – Sagar

2:30pm: Coffee break

3:00pm: Building Software Workloads in FireSim - Albert

3:30pm: Running a FireSim Simulation: Password Strength Checking on a RISC-V SoC with SHA-3 Accelerators and Linux - Albert

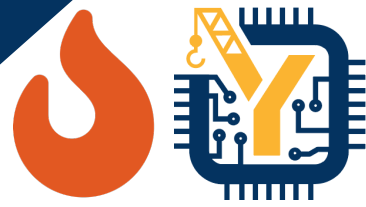
4:00pm: Debugging and Profiling FireSim-Simulated Designs - Abe

4:40pm: FireSim Local (On-Prem) FPGA and Distributed Metasimulation Support - Abe

4:55pm: Conclusion - Sagar

5:00pm: End of Tutorial

Thanks to AWS, Xilinx, and SLICE/ADEPT Lab Sponsors

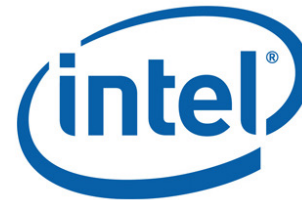


SLICE Lab Sponsors:



National Science Foundation
WHERE DISCOVERIES BEGIN

NSF Award #2016662
CCRI: ENS: Chipyard



Qualcomm



Berkeley Architecture Research