

# FireSim and Chipyard Tutorial: Intro

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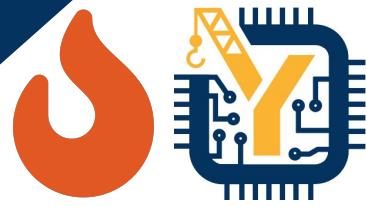
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Berkeley  
Architecture  
Research



# Presenters/Organizers



Sagar  
Karandikar



Jerry  
Zhao



Harrison  
Liew



Abraham  
Gonzalez



Nathan  
Pemberton



Albert  
Ou



Alon  
Amid



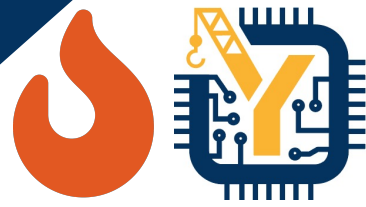
Borivoje  
Nikolić



Krste  
Asanović



# A *Golden Age* in Computer Architecture



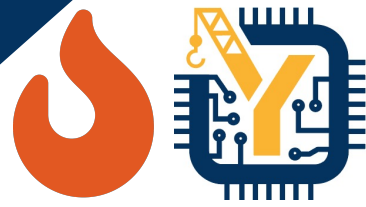
- No more traditional scaling...
- An architect's dream: everyone wants custom microarchitectures and HW/SW co-designed systems
- Also, a golden age to have *direct impact* as researchers
  - Exploding open-source hardware environment
  - An open-ISA that can run software we care about



<https://cacm.acm.org/magazines/2019/2/234352-a-new-golden-age-for-computer-architecture/fulltext>



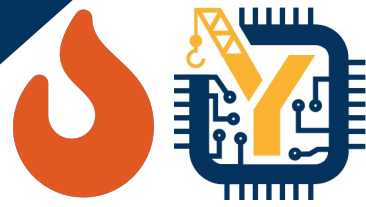
# A *Dark Age* in Computer Architecture tools



- What do we need to do good architecture research?
  - Need tools that let us evaluate designs on a variety of metrics:
    - Functionality
    - Performance
    - Power
    - Area
    - Frequency
  - Especially in small teams (grad students, startups), these tools need to be *agile*
  - Historically, without good open IP, had to build abstract arch/uarch simulators out of necessity
    - But now, we have much better IP and software compatibility, so what's stopping us?



# A *Dark Age* in Computer Architecture tools

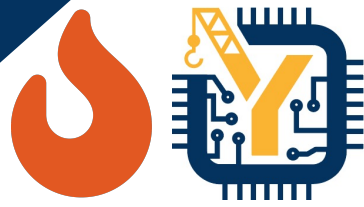


- Designed to be operated by hundreds of engineers
- Not, 10s of engineers or 1s-10s of grad students
- Two hard questions:
  - Where do I get a collection of well-tested hardware IP + complex software stacks that run on it?
  - How do I quickly obtain performance measurements for a novel HW/SW system?





# Two hard questions, answered!



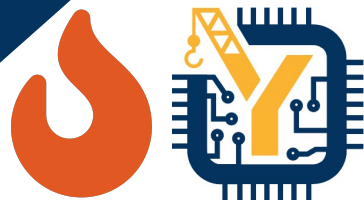
- Where do I get a collection of well-tested hardware IP + complex software stacks that run on it?



- How do I quickly obtain performance measurements for a novel HW/SW system?



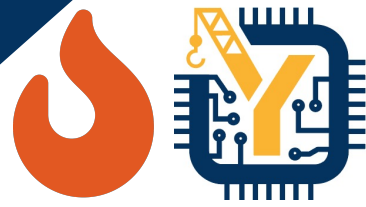
# What can I do with these tools?



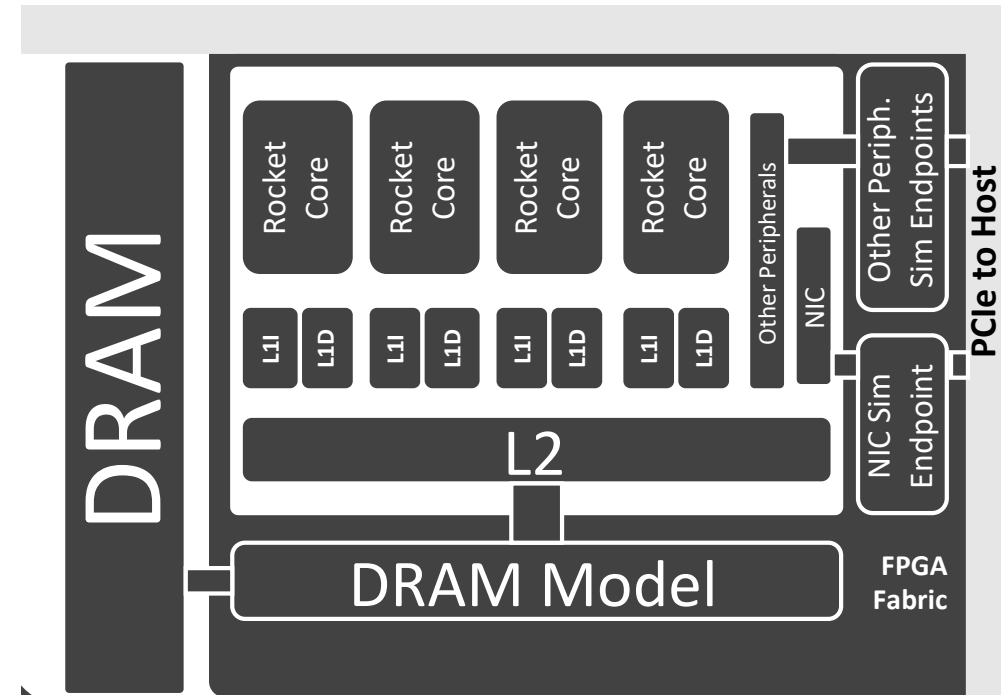
**Measure Functionality, Performance, Power,  
Area, Frequency *for real HW/SW systems,*  
quickly and easily, with small teams of engineers**



# What kinds of designs can I work with?



- RISC-V Cores:
  - Rocket Chip In-Order core, industry proven
  - SonicBOOM Out-of-Order Superscalar core
- Accelerators
  - Hwacha Vector Accelerator
  - sha3 accelerator
  - NVDLA (NVIDIA Deep Learning Accelerator)
  - ML Accelerators (Gemmini)
- Peripherals/other IP
  - L2 Cache, UART, Disk, Ethernet NIC, etc.
- FPGA-Simulation Models
  - Large LLCs, large DDR3 memory systems

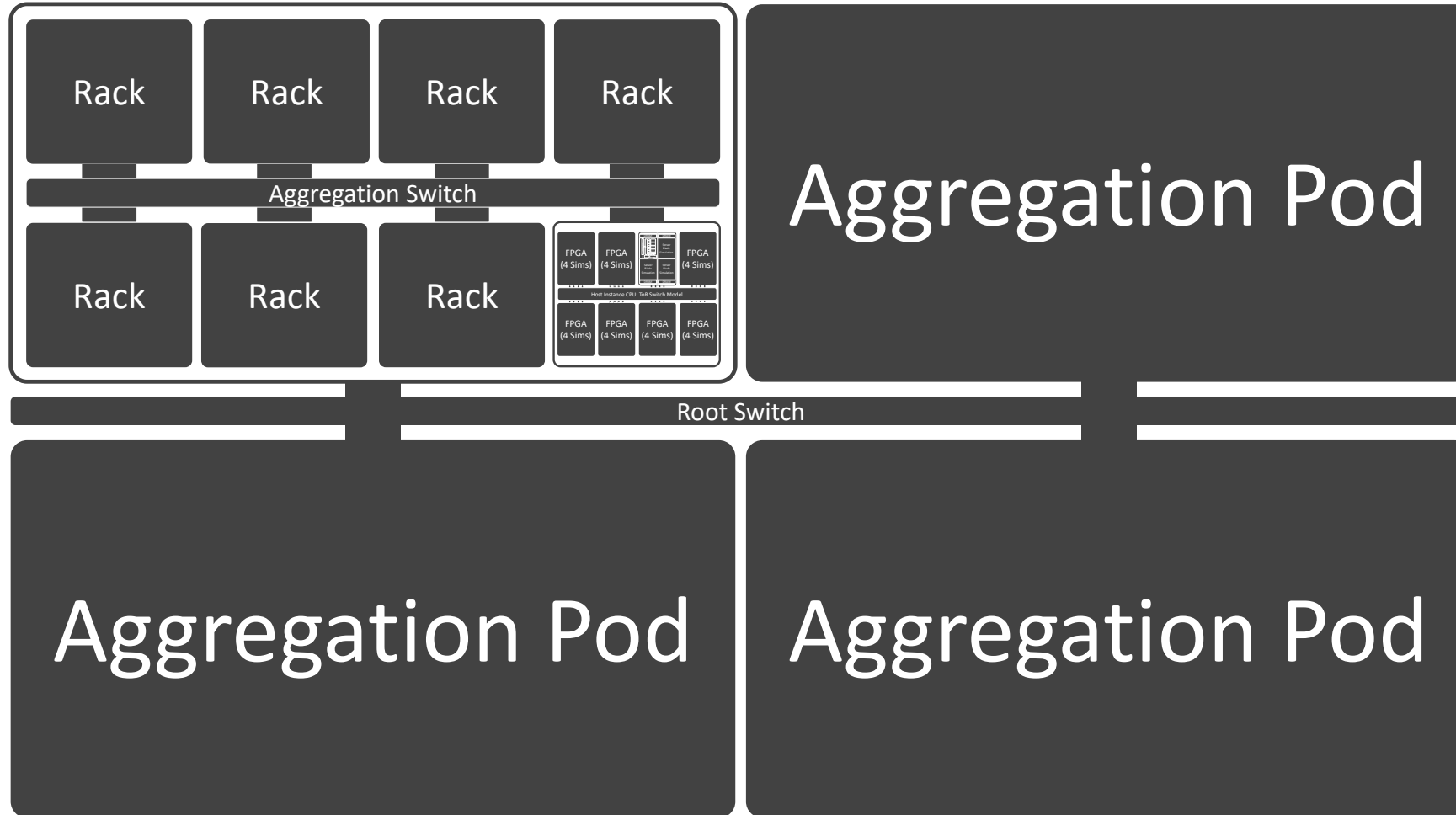
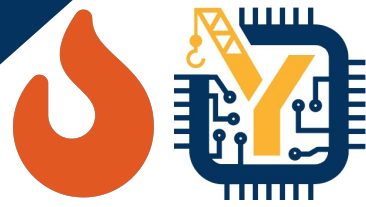


Single SoC System

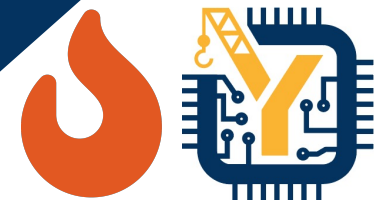




# What kinds of designs can I work with?



# Chipyard is Community-Friendly



## Documentation:

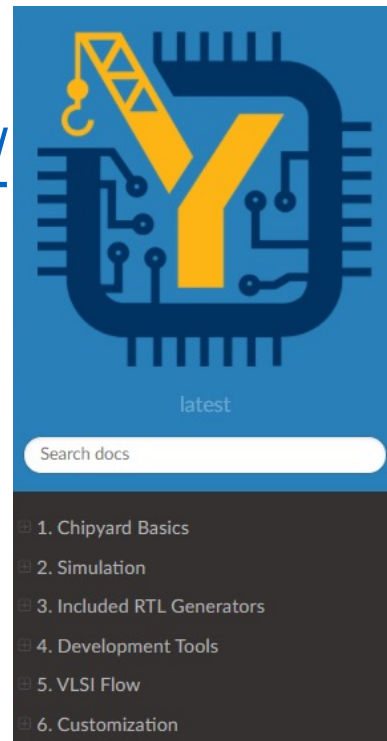
- <https://chipyard.readthedocs.io/en/dev/>
- 133 pages
- Most of today's tutorial content is covered there

## Mailing List:

- [google.com/forum/#!forum/chipyard](https://google.com/forum/#!forum/chipyard)

## Open-sourced:

- All code is hosted on GitHub
- Issues, feature-requests, PRs are welcomed



Docs » Welcome to Chipyard's documentation!

[Edit on GitHub](#)

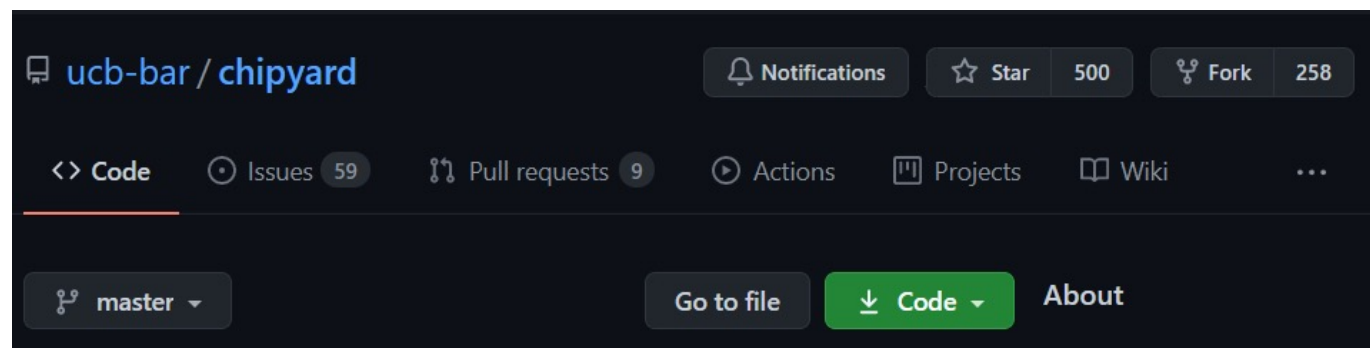
## Welcome to Chipyard's documentation!



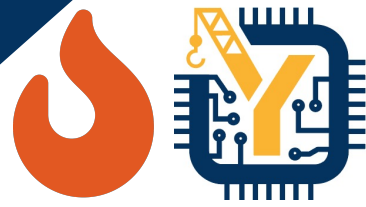
Chipyard is a framework for designing and evaluating full-system hardware using agile teams. It is composed of a collection of tools and libraries designed to provide an integration between open-source and commercial tools for the development of systems-on-chip.

### Important

New to Chipyard? Jump to the [Initial Repository Setup](#) page for setup instructions.



# Growing FireSim Community!

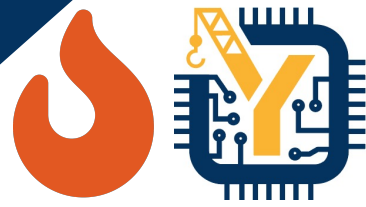


- Companies publicly announced using FireSim
  - Esperanto Maxion ET
  - Intensivate IntenCore
  - SiFive validation paper @ VLSI'20
- Chipyard integration
- Projects with public FireSim support
  - Rocket Chip, BOOM
  - Hwacha Vector Accelerator
  - Keystone Secure Enclave
  - NVIDIA Deep Learning Accelerator (NVDLA)
    - <https://devblogs.nvidia.com/nvdl/>
  - BOOM Spectre replication/mitigation
  - More in-progress! PR yours!
- Many academic users
  - ISCA '18: Maas et. al. HW-GC Accelerator (Berkeley)
  - MICRO '18: Zhang et. al. "Composable Building Blocks to Open up Processor Design" (MIT)
  - RTAS '20: Farshchi et. al. BRU (Kansas)
  - EuroSys '20: Lee et. al. Keystone (Berkeley)
  - OSDI '21: Ibanez et. al. nanoPU (Stanford)
  - See FireSim website for more!
- Education
  - Berkeley CS152/252
  - CCC/RV Summit tutorials
  - MICRO 2019 full-day tutorial
- More than 100 mailing list members
- More than 250 unique cloners per week

*FireSim ISCA'18 paper selected as an **IEEE Micro Top Pick of 2018 Arch. Confs**  
and as the **CACM Research Highlights Nominee from ISCA'18***



# Today's Agenda



09:00: Introduction, logistics, etc. – Sagar

09:05: Chipyard Basics – Jerry

09:35: Customizing the SoC – Jerry

10:05: Integrating Verilog Designs in Chipyard - Abe

## **10:15: Coffee break**

10:25: Hammer VLSI flow – Harrison

10:55: FPGA Prototyping – Abe

11:25: FireSim Introduction – Sagar

## **11:55: Lunch**

12:45: FireSim – Building Hardware Designs - Sagar

13:15: FireSim – Building Software Workloads - Nathan

13:45: Running a FireSim Simulation: Simulating the SHA3 w/Linux - Albert

## **14:15: Coffee break**

14:25: Debugging and Profiling a FireSim-simulated design - Alon

14:50: Conclusion - Alon

